

**REMARKS**

Claims 1-31 are currently pending in the application. Reconsideration of the rejected claims in view of the above amendments and the following remarks is respectfully requested.

***Allowable Claims***

Claims 10, 11, 23 and 24 were indicated to contain allowable subject matter. However, these claims are not being presented in independent form at this time because claims 7 and 20, from which these claims depend, are believed to be allowable. Furthermore, Applicants submit that all of the pending claims are in condition for allowance and that the rejection under § 102 should be withdrawn.

***35 U.S.C. § 102(a) Rejection***

Claims 1-9, 12-22 and 25-31 were rejected under 35 U.S.C. § 102(a) as being anticipated by the Article entitled "Block-based Static Timing Analysis with Uncertainty" by Anirudh DEVGAN et al. This rejection is respectfully traversed.

In order to establish a *prima facie* case of anticipation under 35 U.S.C. § 102, a single prior art reference must disclose each and every element as set forth in the subject claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). Applicants respectfully submit that a *prima facie* case of anticipation has not been established as the applied reference fails to teach each and every element of the claims.

More particularly, independent claims 1 and 14 recite, *inter alia*,

wherein the method predicts a delay in circuit paths by considering a portion of the delay that is influenced by a proximity of circuit elements in a path or paths separately from a full delay distribution.

Additionally, independent claims 7 and 20 recites, *inter alia*,

computing a timing slack for the timing test using the at least one location information, wherein the at least one location information comprises a centroid of the one or more inputs to the timing test.

Furthermore, independent claim 27 recites, *inter alia*,

determining a timing slack variation in the early path using location information on one or more elements in the early path, determining a timing slack variation in the late path using location information on one or more elements in the late path, and, computing a new timing slack for the early path and the late path by using the timing slack variation in the early path and the timing slack variation in the late path.

The applied reference does not teach, or even suggest, at least these features.

Applicants acknowledge that DEVGAN discloses a statistical timing analysis wherein “delay and arrival times in the circuit are modeled as random variables” (see page 608 col. 1, lines 19-21). Applicants also acknowledge that DEVGAN discloses that “critical paths and slack distributions can be computed for a given probability or confidence level” (see page 608, col. 2, lines 9-23). However, it is not apparent that DEVGAN discloses, or even suggests, that the method predicts a delay in circuit paths by considering a portion of the delay that is influenced by a proximity of circuit elements in a path or paths separately from a full delay distribution (claims 1 and 14). Applicants note, in particular, that the Examiner has failed to identify any disclosure in this document indicating that the disclosed analysis even accounts for a proximity of circuit elements in a path or paths, much less, doing so separately from a full delay

distribution.

The Examiner identifies pages 607 and 608 (Introduction section) as teaching the identification of the cause of timing failures in an existing circuit (claims 1, 7, 14, 20 and 27). This assertion is incorrect. The Introduction section merely discusses how circuits can be modeled and/or designed using statistical techniques. In fact, the middle paragraph of col. 1 of page 608 specifically explains that the “[p]arts of the circuit (or gates) can be modeled as deterministic” (emphasis added). The invention, in contrast, specifically provides for designing the circuit based on the analysis of the design, and/or provides for the identification of the cause of timing failures in an existing circuit. An existing circuit is one that is tangible and actually exists and not one that is merely modeled or designed in a computer.

DEVGAN simply does consider the proximity of circuits when analyzing timing. The passage cited and underlined by the examiner on page 8 of the office action relates to the connectivity of circuits, and not their proximity. It is clear from the instant specification that the term proximity as used in the claims refers to physical separation distance on the integrated circuit. The abstract location information as recited in claim 12, for example, is clearly described in the description of our invention as referring to similarities in the characteristics of different gates. DEVGAN is silent on the locations of circuits, much less, the similarities between their characteristics. In fact, the only type of correlation taken into account in DEVGAN relates to reconvergent fanout, in which a single signal is propagated along two separate paths and then recombined in a downstream gate.

Furthermore, while the Examiner has identified page 610, col. 1, lines 6-17 and pages 610-612, section 3 and Fig. 9 as disclosing that the at least one location information comprises a centroid of the one or more inputs to the timing test (claims 7 and 20), it is apparent that the cited language is silent with regard to utilizing in the analysis a centroid of the one or more inputs to the timing test. Nor has the Examiner explained how such language or the drawing of Fig. 9 can be interpreted to disclose or suggest utilizing a centroid of the one or more inputs to the timing test in the analysis. As the Examiner well knows, the centroid referred to in the claimed invention is not a particular set of circuits, as is the "other logic" in DEVGAN (see Fig. 9), but instead is a location in a physical or abstract space.

Moreover, while the Examiner has alleged that DEVGAN discloses determining a timing slack variation in the early path using location information on one or more elements in the early path, determining a timing slack variation in the late path using location information on one or more elements in the late path, and computing a new timing slack for the early path and the late path by using the timing slack variation in the early path and the timing slack variation in the late path (claim 27) at pages 608-610, the Examiner has failed to identify any specific language in this document in support of such assertions. Applicants note, for example, that while the noted language discusses comparing deterministic arrival times and probabilities thereof (see Fig. 3), there is no apparent disclosure or suggestion indicating that both early and late paths are accounted for, much less, that a timing slack variation thereof is utilized in the analysis.

Nor has the Examiner explained how the noted language can be interpreted to disclose or suggest these features.

Applicants emphasize that, as regards an early/late difference, when DEVGAN takes a max function of two delay distributions, this is clearly understood by those of ordinary skill in the art to comprise a late mode analysis. An early mode analysis would have to take min functions of converging path arrival times, and a test between an early and late mode path would have to take a difference between these paths. This is well known in the art, and Applicants are not claiming combined early/late mode analysis by itself. Instead, Applicants have claimed this feature in conjunction with location information to better model the likelihood of timing failure of an early vs. late mode test.

Applicants also emphasize that whereas DEVGAN uses a statistical probability analysis to determine critical paths and slack distributions, the invention, by way of example, uses actual determined information in the timing test.

On pages 7-9 of the instant Office Action, the Examiner identifies certain language of DEVGAN and explains that the noted language discloses predicting a delay in circuit paths by considering a portion of the delay that is influenced by a proximity of circuit elements in a path or paths separately from a full delay distribution (claims 1 and 14), that the at least one location information comprises a centroid of the one or more inputs to the timing test (claims 7 and 20), and determining a timing slack variation in the early path using location information on one or more elements in the early path, determining a timing slack variation in the late path using location information on one or more elements in the late path, and computing a new timing slack for the early path and

the late path by using the timing slack variation in the early path and the timing slack variation in the late path (claim 27).

Such assertions are unsupported by any prior art disclosure. For example, there is no language in DEVGAN explaining that the “other logic” of Fig. 9 is used “for a portion of the delay.” The Examiner has also failed to explain how the noted language, which merely generally discusses how to compute an arrival time at the output of a gate, can be properly interpreted to disclose the recited features which specifically recites predicting a delay in circuit paths by considering a portion of the delay that is influenced by a proximity of circuit elements in a path or paths separately from a full delay distribution (claims 1 and 14), and/or that the at least one location information comprises a centroid of the one or more inputs to the timing test (claims 7 and 20), and/or determining a timing slack variation in the early path using location information on one or more elements in the early path, determining a timing slack variation in the late path using location information on one or more elements in the late path, and computing a new timing slack for the early path and the late path by using the timing slack variation in the early path and the timing slack variation in the late path (claim 27). Applicants remind the Examiner that it is the Examiner who bears the initial burden of establishing how each claim feature is disclosed by the applied reference.

Furthermore, dependent claims 2-6, 12, 13, 15-19, 21, 22, 25, 26, 28, 30 and 31 recite additional features which are not disclosed, or even suggested, by DEVGAN and the Examiner has not shown otherwise.

For example, DEVGAN clearly fails to disclose the logic cone of claims 2 and 15,

the bounding region recited in claims 3-6, 16-19 and 28, and the abstract location information of claims 12, 13, 25 and 26. In particular, whereas DEVGAN teaches determining the information statistically for paths, it is not correct that DEVGAN teaches gathering one set of information for the entire input cone.

Accordingly, Applicants respectfully submit that the rejection under 35 U.S.C. § 102(a) should be withdrawn.

### CONCLUSION

In view of the foregoing remarks, Applicants submit that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicants hereby make a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to Deposit Account No. 09-0456.

Respectfully submitted,  
David J. HATHAWAY et al.



Andrew M. Calderon  
Registration No. 38,093

January 12, 2007  
Greenblum & Bernstein, P.L.C.  
1950 Roland Clarke Place  
Reston, Virginia 20191  
Telephone: 703-716-1191  
Facsimile: 703-716-1180